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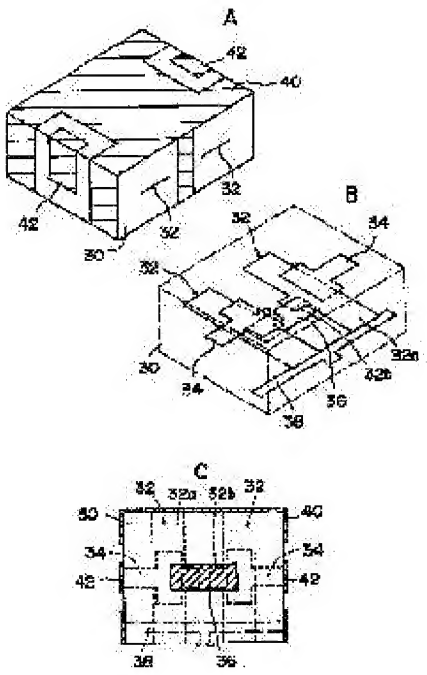
(54) **LAYERED DIELECTRIC FILTER**



(57)Abstract:

PROBLEM TO BE SOLVED: To improve a filter characteristic by inserting attenuating electrode in a prescribed frequency band and shifting an effect that is caused by 1/2 wavelength resonance to a high pass-band side that is higher than three times the wave band.

SOLUTION: This filter is a strip line type layered dielectric filter in which plural resonator inner conductors 32 whose one end is open and the other end is short-circuited and internally inserted input-output electrodes 34 are internally provided inside a dielectric chip 30 in which many dielectric sheets are layered, jointed and sintered integrally, and a resonator outer conductor 40 and external input-output electrodes 42 are provided externally. A resonator inner conductor has a shape, in which a band-shaped pattern 32a that extends from one side of the dielectric chip to the other side and a projecting pattern 32b that is directed towards in the direction of an adjacent resonator inner conductor from its side edge continue, and projecting patterns of the adjacent resonator inner conductors face each other. A rectangular capacitive connecting pattern 34 is embedded in the layered direction of the resonator inner conductor at intervals, so that it overlaps on both projecting patterns and is also connected to them.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the laminated dielectric filter which laminated and sintered many dielectric sheets so that two or more resonator inner conductors might be laid under the inside. The band-like pattern which will be prolonged from one side of a dielectric chip to the side of another side in a resonator inner conductor in this invention if it states in detail, An interval is set to a resonator inner conductor in a laminating direction, and burial arrangement of the pattern for capacitive coupling of rectangular shape is carried out so that it may be considered as the shape which consists of a projection pattern which follows the side edge, and it may lap with the projection pattern in which an adjoining resonator inner conductor faces mutually and between both projection patterns may be connected.
Therefore, it is related with the laminated dielectric filter which has improved the harmonic performance.
This laminated dielectric filter is used in various mobile communications equipment, such as a car telephone which used microwave, for example, and a cellular phone.
[0002]
[Description of the Prior Art]As a filter for microwave which uses dielectric materials, there is form which constitutes a resonator from the strip line. In a 1/4 wavelength resonator type case, one end is an open end, the other end is a short circuit end, one fourth of the strip-line type resonator inner conductors of resonant wavelength of one odd times the length of this are formed in the inside of dielectric materials, and, outside, a resonator outer conductor and an input output electrode are provided. The band-pass filter characteristic is obtained by installing two or more such resonator inner

conductors side by side inside dielectric materials, so that it may become the degree of coupling according to filter characteristics.

[0003]The laminated structure is adopted partly that much more miniaturization is required and a dielectric filter should correspond to it with the miniaturization of communication equipment in recent years. This is manufactured by the method of laminating the dielectric sheet (green sheet) which is not calcinated [many], and carrying out application-of-pressure unification and sintering. For example, an internal resonator inner conductor is formed on a dielectric sheet by screen-stencil of conductive paste, many dielectric sheets including it are laminated, sticking-by-pressure unification is carried out, and a resonator outer conductor and an input output electrode are formed and sintered outside. Usually, after using a big dielectric sheet, carrying out array forming of many required conductive patterns regularly in all directions on it, carrying out the sticking-by-pressure unification of it and considering it as a tabular dielectric block so that many picking can be performed, the process which disconnects the tabular dielectric block in all directions, and is divided into chip shape is adopted.

[0004]An example of the conventional two-step Qom Rhine type filter is shown in drawing 7. B shows the fluoroscopy state of only an internal conductor layer, and C shows the horizontal section in the interpolation input output electrode position for the appearance in the state where A turned the component side upwards, respectively. In order to make a drawing intelligible, also in which figure of an accompanying drawing, the portion which gave parallel lines expresses the conductor layer. Although the conductor layer is drawn quite thickly partly (for example, peripheral part of C of drawing 7, etc.), conductive paste is actually printed by screen-stencil etc., and it prints, and is a **** film.

[0005]The two resonator inner conductors 12 of an other end short circuit are allocated in the inside of the dielectric chip 10 by one end opening, and the resonator outer conductor 14 and the external I/O electrode 16 used as an external ground conductor are formed in the outside surface of the dielectric chip 10. The resonator inner conductor 12 is a band-like pattern, and it is mutually provided in parallel here so that it may reach to the side of another side which counters it from one side of the dielectric chip 10, One end is an opened condition (not connected to the resonator outer conductor 14), and the other end has become a short condition (connected to the resonator outer conductor 14). The two resonator inner conductors 12 are formed so that it may come to the side where each open end is the same.

[0006]The interpolation earth pattern 18 is formed in a layer which is different in this resonator inner conductor 12 in the position by the side of an open end so that it may

intersect perpendicularly with the resonator inner conductor 12, and the end is connected to the resonator outer conductor 14. This interpolation earth pattern 18 is for shortening resonator inner conductor length and attaining much more miniaturization of a dielectric chip. It is a layer which is different in the resonator inner conductor 12, and the pattern 20 for capacitive coupling of rectangular shape is formed so that between both the resonator inner conductors 12 may be connected. It supposes that this pattern 20 for capacitive coupling is equivalent to having inserted the capacitor substantially among both resonator inner conductors, and the function which owner-polarizes a filter and makes a filter damping property good by it is achieved. The external I/O electrode 16 and the flowing interpolation input output electrode 22 are formed. An equivalent circuit is shown in drawing 8. The numerals 24 are the equivalent circuit parts by the pattern for capacitive coupling. The external I/O electrode 16 is installed so that one main table side (A of drawing 7 upper surface) may be followed from a both-ends side.

[0007]As other examples of a dielectric filter, as shown in drawing 9, there is composition formed so that the electrode 26b for capacitive coupling may be projected in the side edge of the band-like pattern 26a as the resonator inner conductor 26. The electrode 26b for capacitive coupling is arranged so that it may approach mutually between the adjoining resonator inner conductors 26. Since a capacitor is formed equivalent of this and an attenuation pole is formed of it, a filter damping property improves.

[0008]

[Problem(s) to be Solved by the Invention]In the composition which forms the electrode 26b for capacitive coupling in the resonator inner conductor 26 as shown in drawing 9 in one, in order to form a capacitor by a flat-surface placed opposite, capacity is small, and in order to earn capacity, the electrode 26b for capacitive coupling must be formed in the open end side of the resonator inner conductor 26. Then, since a chip is miniaturized, when it is going to insert an interpolation earth pattern, the inconvenience to which interference takes place arises. If the electrode for capacitive coupling is enlarged and it is made to approach more, capacity can be earned, but if it does so, combination between original resonators will be affected and the filter-characteristics curve in fundamental wave frequency will collapse.

[0009]Although an attenuation peak can be given outside a pass band by arranging the pattern 20 for capacitive coupling in a different layer to the adjoining resonator inner conductor 12 so that a part may lap, respectively, and a filter damping property can be made good in the laminated dielectric filter of structure as shown in drawing 7, On the

other hand, the pattern for capacitive coupling causes 1/2-wave resonance, and has become a factor which worsens the characteristic in frequency areas, such as a double wave of a fundamental wave, and three double waves, respectively.

[0010]The dielectric filter which uses the pattern for connection capacity as shown in drawing 10 as a step impedance type as a policy which improves the harmonic performance of a filter is proposed. In this dielectric filter, the resonator inner conductor 28 is a band-like pattern, and a flank pattern which the pattern 29 for capacitive coupling is prolonged right-angled to it to the central pattern prolonged in the direction which connects between both resonator inner conductors, and its both ends, and laps with a resonator inner conductor is [the whole] the shape which makes H type continuously. Thus, if the pattern 29 for capacitive coupling is used as a step impedance type, compared with the case of linear shape which is looked at by the conventional example of drawing 7, the electrical length on credit becomes long, and 1/2-wave resonance can be shifted to the low frequency wave side. However, in this technique, there is a possibility that a problem may remain in the frequency area of a double wave or three double waves.

[0011]The purpose of this invention is to provide the laminated dielectric filter which shortens the length of the pattern for capacitive coupling, moves the influence by 1/2-wave resonance to the high region side rather than a wave band region 3 times, and can improve a harmonic performance, securing sufficient connection capacity to put an attenuation pole into a predetermined frequency band. Other purposes of this invention are to provide the laminated dielectric filter of the structure where ease the difference of the lamination thickness by an internal conductive pattern, it is made for the pressure for sticking by pressure to the time of lamination to be further applied to an average, and stabilization of a process can be attained.

[0012]

[Means for Solving the Problem]Two or more resonator inner conductors of an other end short circuit by one end opening with an inside of a dielectric chip in which many dielectric sheets are laminated and joined, and the sintering unification of this invention is carried out, An interpolation input output electrode which sets and counters is laid underground to a resonator inner conductor located in both ends, and an interval in a laminating direction in an outside surface of a dielectric chip. A resonator outer conductor and an external I/O electrode which became independent of this resonator outer conductor are provided, and an end part of said interpolation input output electrode is a strip-line type laminated dielectric filter of structure connected to an external I/O electrode. Said resonator inner conductor is the shape where a band-like

pattern prolonged from one side of a dielectric chip to the side of another side and a projection pattern which goes in the direction of a resonator inner conductor which adjoins from a side edge of this band-like pattern continued, and it is formed so that said projection pattern may face mutually with an adjoining resonator inner conductor. And an interval is set to a resonator inner conductor in a laminating direction, and burial arrangement of the pattern for capacitive coupling of rectangular shape is carried out so that it may lap with said projection pattern in which an adjoining resonator inner conductor faces mutually and between both projection patterns may be connected.

[0013]According to the experiment which this invention person etc. conducted, when a pattern for capacitive coupling was shortened, it has checked that a peak by 1/2-wave resonance moved to the high frequency side in connection with it. Since a pattern for capacitive coupling becomes short, it becomes impossible however, to take connection capacity with a resonator inner conductor. This invention solves the above technical technical problems by learning of this phenomenon, and grasp of a problem accompanying it. That is, it projects to a side edge of a resonator inner conductor, a pattern is provided, and sufficient connection capacity by arranging a pattern for capacitive coupling in a different layer so that it may lap with it to put an attenuation pole into a position can be secured. Since a pattern dimension for capacitive coupling can moreover be shortened, influence by 1/2-wave resonance can be moved to the high region side rather than three double waves, and a harmonic performance is improved by it.

[0014]

[Embodiment of the Invention]In this invention, the pattern for capacitive coupling may be formed so that it may lap with both the band-like pattern of a resonator inner conductor, and an adjoining projection pattern, it may be made shorter than the band-like pattern interval of an adjoining resonator inner conductor, and it may be formed so that it may lap only with a projection pattern. If it forms so that it may lap only with a projection pattern, it is lost that many conductive patterns focus and lap locally inside a dielectric chip, the difference of lamination thickness can be eased, the pressure at the time of lamination can be equalized, and stabilization of a process can be attained. The pattern for capacitive coupling can also be arranged to the upper and lower sides of a laminating direction so that it may provide in one side (the upper part or lower part) of a resonator inner conductor and a resonator inner conductor may be inserted.

[0015]This invention can be applied also to the Qom Rhine type, and can be applied also to an interdigital type. Not only when the number of resonators is two, but in the case of

three or more steps, it is applicable.

[0016]

[Example]Drawing 1 and drawing 2 show one example of the laminated dielectric filter concerning this invention, and are a two-step Qom Rhine type example. B shows the fluoroscopy state of only an internal conductor layer for the appearance in the state where A of drawing 1 turned the component side upwards, and C shows the horizontal section in the pattern position for capacitive coupling. Drawing 2 shows the laminating condition of each dielectric sheet in a laminated dielectric filter.

[0017]The two resonator inner conductors 32 of an other end short circuit are laid under the inside of the dielectric chip 30 by one end opening, an interval is set and the interpolation input output electrode 34 is formed in the one side side (A of drawing 1, and B upper part) of this resonator inner conductor 32. An interval is set, the pattern 36 for capacitive coupling is formed in the opposite side side (A of drawing 1, and B lower part) of the resonator inner conductor 32, and also an interval is set and the interpolation earth pattern 38 is formed in a different layer. The resonator outer conductor 40 and the external I/O electrode 42 used as an external ground conductor are formed in the outside surface of the dielectric chip 30. So that the resonator inner conductor 32 may reach here to the side of another side which counters it from one side of the dielectric chip 30, It is provided mutual almost in parallel, and an end is an opened condition (not connected to the resonator outer conductor 40), and another side has become a short condition (connected to the resonator outer conductor 40). The two resonator inner conductors 32 are formed so that each open ends may serve as the same side (therefore, the side where short circuit ends are the same). The external I/O electrode 42 is the composition (insulated) of having become independent of the resonator outer conductor 40.

It is formed in a different both-ends side from the side with said open end or a short circuit end, and is installed from there to one main table side (A of drawing 1 upper surface).

[0018]The band-like pattern 32a in which the resonator inner conductor 32 is prolonged from one side of a dielectric chip to the side of another side in this invention, It is the shape where the rectangle projection pattern 32b which goes in the direction of a resonator inner conductor which adjoins from the side edge of this band-like pattern 32a continued, and it is provided so that said projection pattern 32b may face mutually with an adjoining resonator inner conductor. the pattern 36 for capacitive coupling -- **** -- it being simple rectangular shape (shape which does not have a swollen part in both

ends), and, An interval is set and arranged to the resonator inner conductor 32 in a laminating direction so that it may lap with said projection pattern 32b of the adjoining resonator inner conductor 32 which faces mutually and between both projection patterns 32b may be connected. The feature of this invention is at this point.

[0019]The interpolation earth pattern 38 is a position of open end slippage of the resonator inner conductor 32, and it provides in a line so that it may connect the both-ends face-to-face of the dielectric chip 30, and it is provided so that the side which has an open end of the resonator inner conductor 32 from the center may be arrived at, and it is connected to the resonator outer conductor 40 at these three ends, respectively. This interpolation earth pattern 38 is for shortening resonator inner conductor length and attaining much more miniaturization of a dielectric chip.

[0020]The interpolation input output electrode 34 is the T shape which carries out contiguity opposite with a large area to the resonator inner conductor 32 continuously with the external I/O electrode 42 by an end.

Input/output coupling capacity is increased by this and the function which strengthens first rank combination (combination with the resonator inner conductor and external I/O electrode which are located in both ends) is achieved.

[0021]Such a laminated dielectric filter can be manufactured in a lamination procedure as shown, for example in drawing 3. The dielectric sheet (green sheet) which is not calcinated [many] is prepared first. They add an organic binder to the dielectric materials for microwave (for example, low-temperature-sintering material which added the glass material to the BaO-TiO_2-Nd_2O_3 system high dielectric constant material), fabricate it to a sheet shaped, and are usually about tens of micrometers in thickness. The dielectric sheet which used conductive paste (for example, silver paste) other than the mere dielectric sheet (dielectric sheet which does not form the conductor layer) 50, and formed the conductive pattern required for the surface with screen printing is prepared. In them. On the whole surface, an outside earth pattern. The dielectric sheet 51 and interpolation earth pattern which were printed. The dielectric sheet 52 and the pattern for capacitive coupling which were printed. The printed dielectric sheet 53, the dielectric sheet 54 which printed the resonator inner conductor, the dielectric sheet 55 which printed the interpolation input output electrode and an outside earth pattern, and it have the dielectric sheet 56 which printed two external I/O electrode patterns insulated to both ends.

[0022]An outside earth pattern and it arrange the dielectric sheet 56 which printed two external I/O electrode patterns insulated to both ends at the bottom, The dielectric

sheet 55 which printed the interpolation input output electrode on it, the dielectric sheet 54 which printed the resonator inner conductor, the dielectric sheet 53 which printed the pattern for capacitive coupling, and the dielectric sheet 52 which printed the interpolation earth pattern, It puts in the order and the dielectric sheet 51 which printed the outside earth pattern on the whole surface is arranged in the topmost part. Among each of above-mentioned dielectric sheets, the required number-of-sheets lamination intervention of the mere dielectric sheet (sheet in which the conductive pattern is not printed) 50 is carried out if needed. However, the lowermost dielectric sheet 56 is laminated by the direction to which an outside earth pattern and an external I/O electrode pattern appear in the lateral surface (drawing 2 undersurface). And sticking-by-pressure unification is carried out by pressurizing the whole. Then, a laminated dielectric filter is obtained by printing and sintering the electrical conducting material used as a resonator outer conductor and an external I/O electrode to the side and the end face of a chip. Actually, a large number are taken using a big dielectric sheet, and it manufactures by a method, and after sticking-by-pressure unification, it will cut in all directions and will sinter.

[0023]Since the fundamental operation as a dielectric filter is the same as that of publicly known conventional technology, the explanation about it is omitted. An equivalent circuit is also the same with being shown in drawing 7 (of course, a circuit constant differs from elegance conventionally). In this invention, it projects to the side edge of the band-like pattern 32a of the resonator inner conductor 32, and the pattern 32b is formed, in order to arrange the pattern 36 for capacitive coupling in a different layer so that it may lap with it, required connection capacity can be secured and an attenuation pole can be put into a predetermined frequency area. And since the pattern dimension for capacitive coupling can be shortened, the influence by 1/2-wave resonance can be moved to the high region side rather than three double waves, and a harmonic performance is substantially improved by it. As for the length of the pattern for capacitive coupling, in this invention, it is preferred to make it shorter than the center line interval of the band-like pattern of an adjoining resonator inner conductor.

[0024]The comparison of a filter pass characteristic (S_{21}) with elegance (structure shown in drawing 7) is shown in drawing 8 this invention article (structure shown in drawing 1), and conventionally. A solid line is the characteristic of this invention article, and a dashed line is the characteristic of elegance conventionally. In conventional technology, since the peak by 1/2-wave resonance appears near a double wave ($2xf_0$), attenuation cannot be taken. Since connection capacity sufficient in this invention article is securable to it, it turns out that it can be made to move to the high frequency side, and

the harmonic performance is substantially improved by it rather than three double waves ($3xf_0$) in the peak by 1/2-wave resonance, the attenuation pole by the side of low-pass presupposing that it is conventionally equivalent to elegance.

[0025]Drawing 4 is an explanatory view showing other examples of the laminated dielectric filter concerning this invention, A shows the horizontal section in the pattern position for capacitive coupling, and B shows the section in the x-x position. Since it is the same as that of said example except pattern 60 for capacitive coupling, identical codes are given to a corresponding portion and the explanation about them is omitted. Some patterns for capacitive coupling were long, in said example, have arranged so that it may lap with both the band-like pattern 32a of the resonator inner conductor 32, and the adjoining projection pattern 32b, but. The pattern 60 for capacitive coupling of this example is made shorter than the band-like pattern interval of the adjoining resonator inner conductor 32, and it is arranged so that it may lap only with the projection pattern 32b.

[0026]If it does in this way, the influence by the part and 1/2-wave resonance to which the pattern 60 for capacitive coupling becomes short will shift to the high frequency side further. Even if it sees the lap of the conductor layer inside a dielectric chip in which position, it becomes below two-layer, so that the section of B of drawing 4 may also show. Therefore, a lamination difference can be eased, a pressure can take much more now for an average at the time of lamination, the reliability of sticking by pressure between dielectric sheets can be raised, and stabilization of a process can be attained.

[0027]Drawing 5 is a sectional view of the example of further others of the laminated dielectric filter concerning this invention. Since it is the same as that of said example except pattern 62 for capacitive coupling, identical codes are given to a corresponding portion and the explanation about them is omitted. The pattern 62 for capacitive coupling is arranged to the upper and lower sides of a laminating direction so that it may be made shorter than the band-like pattern interval of the adjoining resonator inner conductor 32 like the example of drawing 4, and may be made to lap only with the projection pattern 32b and the resonator inner conductor 32 may be inserted. Such composition is effective when connection capacity runs short with composition as shown in drawing 4.

[0028]This invention is applicable not only to the above Qom Rhine types but an interdigital type filter. An example in the case of a two-step interdigital type filter is shown in drawing 6. B shows the fluoroscopy state of only an internal conductor layer for the appearance in the state where A turned the component side upwards, and C shows the horizontal section in the pattern position for capacitive coupling.

[0029]The two resonator inner conductors 72 of an other end short circuit are laid under the inside of the dielectric chip 70 by one end opening, an interval is set and the interpolation input output electrode 74 is formed in the one side side (A of drawing 6, and B upper part) of this resonator inner conductor 72. An interval is set to the opposite side side (A of drawing 6, and B lower part) of the resonator inner conductor 72, and the pattern 76 for capacitive coupling is formed. The resonator outer conductor 80 used as an external ground conductor and the external I/O electrode 82 are formed in the outside surface of the dielectric chip 70. So that the resonator inner conductor 72 may reach here to the side of another side which counters it from one side of the dielectric chip 70, It is provided mutual almost in parallel, and an end is an opened condition (not connected to the resonator outer conductor 80), and another side has become a short condition (connected to the resonator outer conductor 80). The two resonator inner conductors 72 are formed so that an open end and a short circuit end may become reverse mutually (that is, it becomes alternate like). The external I/O electrode 82 is formed in a different both-ends side from the side with said open end or a short circuit end, and is installed from there to one main table side (A of drawing 6 upper surface).

[0030]The band-like pattern 72a in which the resonator inner conductor 72 is prolonged from one side of the dielectric chip 70 to the side of another side, It is the shape where the projection pattern 72b which goes in the direction of a resonator inner conductor which adjoins from the side edge of this band-like pattern 72a continued, and it is provided so that it may project with an adjoining resonator inner conductor and the pattern 72b may face mutually. the pattern 76 for capacitive coupling -- **** -- it is simple rectangular shape, and an interval is set and arranged to a resonator inner conductor in a laminating direction so that it may lap with said projection pattern 72b in which the adjoining resonator inner conductor 72 faces mutually and between both projection patterns 72b may be connected.

[0031]The interpolation input output electrode 74 is the T shape which carries out contiguity opposite with a large area to the resonator inner conductor 72 continuously with the external I/O electrode 82 by an end.

Input/output coupling capacity is increased by this and the function which strengthens first rank combination (combination with the resonator inner conductor and external I/O electrode which are located in both ends) is achieved.

[0032]Although each of above-mentioned examples [each of] is examples of 2 stage filters which installed two resonator inner conductors side by side, it cannot be overemphasized that this invention is applicable also to three or more steps of filters.

Although provided in the middle position of the band-like pattern of a resonator inner conductor, the pattern for capacitive coupling and a projection pattern can be shifted you to be not only it but ****** et al., and may be arranged. For example, if it shifts to the open end side, the tendency which the improvement in the characteristic in 3 double wave regions produces will be seen.

[0033]

[Effect of the Invention]This invention is arranging the pattern for capacitive coupling in a different layer so that it may project to the side edge of a resonator inner conductor, a pattern's may be provided as mentioned above and it may lap with it, Since the pattern dimension for capacitive coupling is shortened securing connection capacity required in order to put an attenuation pole into a position, the influence by 1/2-wave resonance can be moved to the high region side rather than three double waves, and a harmonic performance can be substantially improved by it.

[0034]If it arranges in one side so that the pattern for capacitive coupling may be made shorter than the band-like pattern interval of an adjoining resonator inner conductor and it may lap only with a projection pattern, Inside a dielectric chip, since it becomes below two-layer and a lamination difference is eased even if it sees in which position, the lap of a conductor layer can spend much more now for a pressure to an average at the time of lamination, can raise the reliability of sticking by pressure between dielectric sheets, and can attain stabilization of a process.

[Translation done.]

CLAIMS

[Claim(s)]

[Claim 1]Two or more resonator inner conductors of an other end short circuit by one end opening with an inside of a dielectric chip in which many dielectric sheets are laminated and joined, and sintering unification is carried out, An interpolation input output electrode which sets and counters is laid underground to a resonator inner conductor located in both ends, and an interval in a laminating direction in an outside surface of a dielectric chip. In a strip-line type laminated dielectric filter of structure where a resonator outer conductor and an external I/O electrode which became independent of this resonator outer conductor are provided, and an end part of said interpolation input output electrode is connected to an external I/O electrode, A band-like pattern in which said resonator inner conductor is prolonged from one side of a dielectric chip to the side of another side, It is the shape where a projection pattern which goes in the direction of a resonator inner conductor which adjoins from a side edge of this band-like pattern continued, So that it may lap with said projection pattern in which it is provided and an adjoining resonator inner conductor faces mutually so that said projection pattern may face mutually with an adjoining resonator inner conductor and between both projection patterns may be connected, A laminated dielectric filter having set an interval to a resonator inner conductor in a laminating direction, and carrying out burial arrangement of the pattern for capacitive coupling of rectangular shape.

[Claim 2]The laminated dielectric filter according to claim 1 which makes a pattern for capacitive coupling length which laps with both a band-like pattern of a resonator inner conductor, and an adjoining projection pattern.

[Claim 3]The laminated dielectric filter according to claim 1 made into length which

makes a pattern for capacitive coupling shorter than a band-like pattern interval of an adjoining resonator inner conductor, and laps only with a projection pattern.

[Claim 4]The laminated dielectric filter according to claim 2 or 3 which arranges a pattern for capacitive coupling to the upper and lower sides of a laminating direction so that a resonator inner conductor may be inserted.

[Translation done.]

CLAIMS

[Claim(s)]

[Claim 1]Two or more resonator inner conductors of an other end short circuit by one end opening with an inside of a dielectric chip in which many dielectric sheets are laminated and joined, and sintering unification is carried out, An interpolation input output electrode which sets and counters is laid underground to a resonator inner conductor located in both ends, and an interval in a laminating direction in an outside surface of a dielectric chip. In a strip-line type laminated dielectric filter of structure where a resonator outer conductor and an external I/O electrode which became independent of this resonator outer conductor are provided, and an end part of said interpolation input output electrode is connected to an external I/O electrode, A band-like pattern in which said resonator inner conductor is prolonged from one side of a dielectric chip to the side of another side, It is the shape where a projection pattern which goes in the direction of a resonator inner conductor which adjoins from a side edge of this band-like pattern continued, So that it may lap with said projection pattern in which it is provided and an adjoining resonator inner conductor faces mutually so that said projection pattern may face mutually with an adjoining resonator inner conductor and between both projection patterns may be connected, A laminated dielectric filter having set an interval to a resonator inner conductor in a laminating direction, and carrying out burial arrangement of the pattern for capacitive coupling of rectangular shape.

[Claim 2]The laminated dielectric filter according to claim 1 which makes a pattern for capacitive coupling length which laps with both a band-like pattern of a resonator inner conductor, and an adjoining projection pattern.

[Claim 3]The laminated dielectric filter according to claim 1 made into length which

makes a pattern for capacitive coupling shorter than a band-like pattern interval of an adjoining resonator inner conductor, and laps only with a projection pattern.

[Claim 4]The laminated dielectric filter according to claim 2 or 3 which arranges a pattern for capacitive coupling to the upper and lower sides of a laminating direction so that a resonator inner conductor may be inserted.

[Translation done.]

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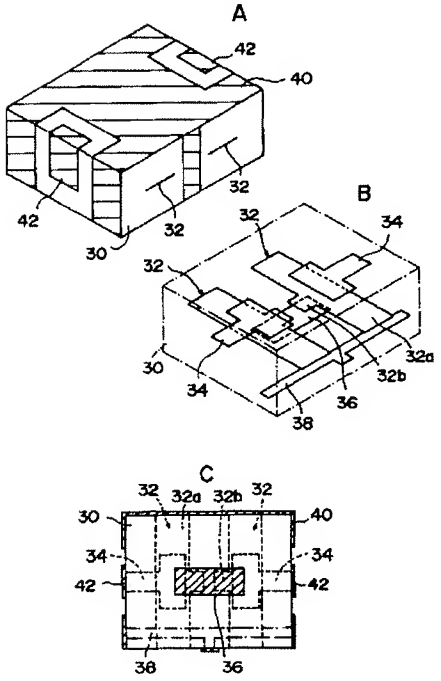
(54)【発明の名称】積層誘電体フィルタ

(57)【要約】

【課題】　所定の周波数帯域に減衰極を入れる、且つ1／2波長共振による影響を3倍波帯域よりも高域側に移動させて、フィルタ特性を改善する。

【解決手段】　多数の誘電体シートが積層・接合されて焼結一体化されている誘電体チップ30の内部に、一端開放で他端短絡の複数の共振器内導体32と、内挿入出力電極34が埋設され、外面には共振器外導体40と外部入出力電極42とが設けられるストリップ線路型積層誘電体フィルタである。共振器内導体は、誘電体チップの一方の側面から他方の側面まで延びる帯状パターン32aと、その側縁から隣接する共振器内導体方向に向かう突出パターン32bとが連続した形状であって、隣接する共振器内導体で突出パターンが互いに向き合うように設ける。両突出パターンと重なり且つそれらを連絡するように、共振器内導体に対して積層方向で間隔をおいて矩形状の容量結合用パターン34を埋設する。



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【特許請求の範囲】

【請求項１】　多数の誘電体シートが積層・接合されて焼結一体化されている誘電体チップの内部に、一端開放で他端短絡の複数の共振器内導体と、両端に位置する共振器内導体に対して積層方向で間隔をおいて対向する内挿入出力電極が埋設され、誘電体チップの外面には、共振器外導体と、該共振器外導体から独立した外部入出力電極とが設けられ、前記内挿入出力電極の一端部が外部入出力電極に接続される構造のストリップ線路型の積層誘電体フィルタにおいて、

前記共振器内導体は、誘電体チップの一方の側面から他方の側面まで延びる帯状パターンと、該帯状パターンの側縁から隣接する共振器内導体方向に向かう突出パターンとが連続した形状であって、隣接する共振器内導体で前記突出パターンが互いに向き合うように設けられ、隣接する共振器内導体の互いに向き合う前記突出パターンと重なり且つ両方の突出パターン間を連絡するように、共振器内導体に対して積層方向で間隔をおいて矩形状の容量結合用パターンを埋設配置したことを特徴とする積層誘電体フィルタ。

【請求項２】　容量結合用パターンを、隣接する共振器内導体の帯状パターン及び突出パターンの両方と重なる長さにする請求項１記載の積層誘電体フィルタ。

【請求項３】　容量結合用パターンを、隣接する共振器内導体の帯状パターン間隔よりも短くし、突出パターンのみと重なる長さにする請求項１記載の積層誘電体フィルタ。

【請求項４】　容量結合用パターンを、共振器内導体を挟むように、積層方向の上下に配置する請求項２又は３記載の積層誘電体フィルタ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、内部に複数の共振器内導体が埋設されるように誘電体シートを多数積層して焼結した積層誘電体フィルタに関するものである。更に詳しく述べると本発明は、共振器内導体を、誘電体チップの一方の側面から他方の側面まで延びる帯状パターンと、その側縁に連続する突出パターンとからなる形状とし、隣接する共振器内導体の互いに向き合う突出パターンと重なり且つ両方の突出パターン間を連絡するように、共振器内導体に対して積層方向で間隔をおいて矩形状の容量結合用パターンを埋設配置することにより、高調波特性を改善した積層誘電体フィルタに関するものである。この積層誘電体フィルタは、例えばマイクロ波を利用した自動車電話や携帯電話などの各種移動体通信機器中で使用される。

【０００２】

【従来の技術】誘電体材料を使用するマイクロ波用フィルタとして、共振器をストリップ線路で構成する形式がある。１／４波長共振器型の場合には、誘電体材料の内

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部に、一端が開放端であり他端が短絡端であって、共振波長の１／４の奇数倍の長さのストリップ線路型の共振器内導体を設け、外面には共振器外導体と入出力電極を設ける。誘電体材料の内部で、このような共振器内導体を複数個、フィルタ特性に応じた結合度となるように並設することによって、帯域通過フィルタ特性が得られる。

【０００３】近年の通信機器の小形化に伴い、誘電体フィルタも一層の小形化が要求され、それに対応すべく一部で積層構造が採用されている。これは、多数の未焼成の誘電体シート（グリーンシート）を積層して加圧一体化し焼結する方法によって製造する。例えば、内部の共振器内導体を、導体ペーストのスクリーン印刷によって誘電体シート上に形成し、それを含めて誘電体シートを多数積層して圧着一体化し、外面に共振器外導体と入出力電極を形成して焼結する。通常、多数個取りができるように、大きな誘電体シートを使用して、その上に多数の必要な導体パターンを縦横規則的に配列形成し、それを圧着一体化して板状誘電体ブロックとした後に、その板状誘電体ブロックを縦横に切断してチップ状に分離する製法が採用されている。

【０００４】従来の２段コムライン型フィルタの一例を図７に示す。Ａは実装面を上に向けた状態での外観を、Ｂは内部の導体層のみの透視状態を、Ｃは内挿入出力電極位置での水平断面を、それぞれ示している。なお図面を分かり易くするために、添付図面のいずれの図においても、平行線を施した部分は導体層を表している。一部で（例えば図７のＣの外周部分などで）導体層をかなり厚く描いてあるが、実際にはスクリーン印刷などにより導体ペーストを印刷し、焼き付けたものであって、極く薄い層である。

【０００５】誘電体チップ１０の内部に、一端開放で他端短絡の２個の共振器内導体１２を配設し、誘電体チップ１０の外表面に外部アース導体となる共振器外導体１４と外部入出力電極１６を形成する。ここで、共振器内導体１２は帯状のパターンであって、誘電体チップ１０の一方の側面からそれに対向する他方の側面まで達するように互いに平行に設けられ、一端が開放状態（共振器外導体１４に接続されない）であって、他端が短絡状態（共振器外導体１４に接続される）となっている。２個の共振器内導体１２は、それぞれの開放端が同じ側面にくるように設けられている。

【０００６】共振器内導体１２と直交するように開放端側の位置に、該共振器内導体１２とは異なる層に内挿アースパターン１８を設け、その端部を共振器外導体１４に接続する。この内挿アースパターン１８は、共振器内導体長さを短縮して誘電体チップのより一層の小形化を図るためのものである。また共振器内導体１２とは異なる層で、両共振器内導体１２間を連絡するように、矩形状の容量結合用パターン２０を設ける。この容量結合用

パターン２０は、両方の共振器内導体間に実質的にコンデンサを挿入したのと等価とし、それによってフィルタを有極化してフィルタ減衰特性を良好にする機能を果たす。更に外部入出力電極１６と導通する内挿入出力電極２２を設ける。等価回路を図８に示す。符号２４が、容量結合用パターンによる等価回路部分である。なお外部入出力電極１６は、両端面から一方の主表面（図７のＡでは上面）に連続するように延設されている。

【０００７】誘電体フィルタの他の例としては、図９に示すように、共振器内導体２６として帯状パターン２６ａの側縁に容量結合用電極２６ｂを突出するように形成する構成がある。容量結合用電極２６ｂは、隣接する共振器内導体２６間で互いに接近するように配置する。これによって等価的にコンデンサが形成され、それによって減衰極が形成されるため、フィルタ減衰特性が向上する。

【０００８】

【発明が解決しようとする課題】図９に示すような共振器内導体２６に容量結合用電極２６ｂを一体的に設ける構成では、平面対向配置でコンデンサを形成するために容量が小さく、容量を稼ぐためには容量結合用電極２６ｂを共振器内導体２６の開放端側に設けなければならない。すると、チップを小形化するために内挿アースパターンを挿入しようとしたときに干渉が起こる不都合が生じる。容量結合用電極を大きくし、より接近させれば、容量を稼ぐことができるが、そうすると、本来の共振器間の結合に影響を与え、基本波周波数でのフィルタ特性曲線がくずれてしまう。

【０００９】また図７に示すような構造の積層誘電体フィルタでは、隣接する共振器内導体１２に対して、それぞれ一部が重なるように異層に容量結合用パターン２０を配置することで、通過帯域外に減衰ピークをもたせることができ、フィルタ減衰特性を良好にできるが、反面、容量結合用パターンが１／２波長共振を起こし、それぞれ基本波の２倍波、３倍波などの周波数域での特性を悪化させる要因となっている。

【００１０】フィルタの高調波特性を改善する方策として、図１０に示すような結合容量用パターンをステップインピーダンス型にする誘電体フィルタが提案されている。この誘電体フィルタでは、共振器内導体２８は帯状パターンであり、それに対して容量結合用パターン２９は、両共振器内導体間を繋ぐ方向に延びる中央パターンとその両端に直角に延びて共振器内導体に重なるような側部パターンとが連続し、全体がＨ型をなす形状である。このように容量結合用パターン２９をステップインピーダンス型にすると、図７の従来例に見られるような直線状の場合に比べて見掛け上の電気的長さが長くなり、１／２波長共振を低周波側にずらすことができる。しかし、この手法では、２倍波あるいは３倍波の周波数域に問題が残る恐れがある。

【００１１】本発明の目的は、所定の周波数帯域に減衰極を入れるために十分な結合容量を確保しながら、容量結合用パターンの長さを短くして、１／２波長共振による影響を３倍波帯域よりも高域側に移動させて高調波特性を改善できる積層誘電体フィルタを提供することである。また本発明の他の目的は、内部の導体パターンによる積層厚さの差を緩和して、積層時に圧着のための圧力がより一層平均にかかるようにし、工程の安定化を図ることができる構造の積層誘電体フィルタを提供することである。

【００１２】

【課題を解決するための手段】本発明は、多数の誘電体シートが積層・接合されて焼結一体化されている誘電体チップの内部に、一端開放で他端短絡の複数の共振器内導体と、両端に位置する共振器内導体に対して積層方向で間隔をおいて対向する内挿入出力電極が埋設され、誘電体チップの外面には、共振器外導体と、該共振器外導体から独立した外部入出力電極とが設けられ、前記内挿入出力電極の一端部が外部入出力電極に接続される構造のストリップ線路型の積層誘電体フィルタである。前記共振器内導体は、誘電体チップの一方の側面から他方の側面まで延びる帯状パターンと、該帯状パターンの側縁から隣接する共振器内導体方向に向かう突出パターンとが連続した形状であって、隣接する共振器内導体で前記突出パターンが互いに向き合うように設ける。そして、隣接する共振器内導体の互いに向き合う前記突出パターンと重なり且つ両方の突出パターン間を連絡するように、共振器内導体に対して積層方向で間隔をおいて矩形状の容量結合用パターンを埋設配置する。

【００１３】本発明者等が行った実験によれば、容量結合用パターンを短くしていくと、それに伴って１／２波長共振によるピークが高周波側へ移動していくことが確認できた。但し、容量結合用パターンが短くなるために、共振器内導体との結合容量がとれなくなる。本発明は、かかる現象の知得と、それに伴う問題点の把握により、上記のような技術的課題を解決したものである。即ち、共振器内導体の側縁に突出パターンを設け、それと重なるように異層に容量結合用パターンを配置することで、所定の位置に減衰極を入れるために十分な結合容量を確保できる。その上、容量結合用パターン寸法を短くできるため、１／２波長共振による影響を３倍波よりも高域側に移動させることができ、それによって高調波特性が改善される。

【００１４】

【発明の実施の形態】本発明において容量結合用パターンは、隣接する共振器内導体の帯状パターン及び突出パターンの両方と重なるように形成してもよいし、隣接する共振器内導体の帯状パターン間隔よりも短くし、突出パターンのみと重なるように形成してもよい。突出パターンのみと重なるように形成すると、誘電体チップの内

部で局所的に多くの導体パターンが集中して重なることがなくなり、積層厚さの差が緩和されて積層時の圧力を平均化でき、工程の安定化を図ることができる。なお容量結合用パターンは、共振器内導体の片側（上方又は下方）に設けてもよいし、共振器内導体を挟むように、積層方向の上下に配置することも可能である。

【００１５】なお本発明は、コムライン型にも適用できるし、インターデジタル型にも適用できる。共振器が2段の場合のみならず、3段以上の場合にも適用できる。

【００１６】

【実施例】図１及び図２は本発明に係る積層誘電体フィルタの一実施例を示しており、２段コムライン型の一例である。図１のＡは実装面を上に向けた状態での外観を、Ｂは内部の導体層のみの透視状態を示し、Ｃは容量結合用パターン位置での水平断面を示している。また図２は積層誘電体フィルタにおける各誘電体シートの積層状態を示している。

【００１７】誘電体チップ３０の内部に一端開放で他端短絡の２個の共振器内導体３２を埋設し、該共振器内導体３２の片面側（図１のＡ，Ｂでは上方）に間隔をおいて内挿入出力電極３４を設ける。共振器内導体３２の反対面側（図１のＡ，Ｂでは下方）に間隔をおいて容量結合用パターン３６を設け、更に間隔をおいて異層に内挿アースパターン３８を設ける。また誘電体チップ３０の外表面に、外部アース導体となる共振器外導体４０と外部入出力電極４２を形成する。ここで共振器内導体３２は、誘電体チップ３０の一方の側面からそれに対向する他方の側面まで達するように、互いにほぼ平行に設けられ、一端が開放状態（共振器外導体４０に接続されていない）であって、他方が短絡状態（共振器外導体４０に接続されている）となっている。２個の共振器内導体３２は、それぞれの開放端同士が同じ側面（従って、短絡端同士も同じ側面）となるように設けられる。外部入出力電極４２は、共振器外導体４０から独立した（絶縁された）構成であり、前記開放端あるいは短絡端のある側面とは異なる両端面に形成され、そこから一方の主表面（図１のＡでは上面）まで延設されている。

【００１８】本発明では、共振器内導体３２は、誘電体チップの一方の側面から他方の側面まで延びる帯状パターン３２ａと、該帯状パターン３２ａの側縁から隣接する共振器内導体方向に向かう矩形突出パターン３２ｂとが連続した形状であって、隣接する共振器内導体で前記突出パターン３２ｂが互いに向き合うように設けられる。容量結合用パターン３６は、極く単純な矩形状（両端に膨出部分をもたない形状）であって、隣接する共振器内導体３２の互いに向き合う前記突出パターン３２ｂと重なり且つ両方の突出パターン３２ｂの間を連絡するように、共振器内導体３２に対して積層方向で間隔をおいて配置する。この点に本発明の特徴がある。

【００１９】内挿アースパターン３８は、共振器内導体３２の開放端寄りの位置で、誘電体チップ３０の両端面間を結ぶように線状に設けると共に、その中央から共振器内導体３２の開放端のある側面に達するように設け、それら３箇所の端部でそれぞれ共振器外導体４０に接続する。この内挿アースパターン３８は、共振器内導体長さを短縮して誘電体チップのより一層の小形化を図るためのものである。

【００２０】内挿入出力電極３４は、一端で外部入出力電極４２と連続し、共振器内導体３２に対して大面積で近接対向するようなＴ型状であり、これによって入出力結合容量を増大させ、初段結合（両端に位置する共振器内導体と外部入出力電極との結合）を強くする機能を果たす。

【００２１】このような積層誘電体フィルタは、例えば図３に示すような積層手順で製造することができる。まず多数の未焼成の誘電体シート（グリーンシート）を用意する。それらはマイクロ波用誘電体材料（例えば、$BaO-TiO_2-Nd_2O_3$系高誘電率材料にガラス材料を添加した低温焼結材料）に有機バインダを加えてシート状に成形したものであり、通常数十μｍ程度の厚さである。単なる誘電体シート（導体層を形成していない誘電体シート）５０の他に、導体ペースト（例えば銀ペースト）を用いてスクリーン印刷法により表面に必要な導体パターンを形成した誘電体シートを用意する。それらには、全面に外面アースパターンを印刷した誘電体シート５１、内挿アースパターンを印刷した誘電体シート５２、容量結合用パターンを印刷した誘電体シート５３、共振器内導体を印刷した誘電体シート５４、内挿入出力電極を印刷した誘電体シート５５、及び外面アースパターンとそれとは絶縁されている２個の外部入出力電極パターンを両端部に印刷した誘電体シート５６がある。

【００２２】最下部に外面アースパターンとそれとは絶縁されている２個の外部入出力電極パターンを両端部に印刷した誘電体シート５６を配置し、その上に内挿入出力電極を印刷した誘電体シート５５、共振器内導体を印刷した誘電体シート５４、容量結合用パターンを印刷した誘電体シート５３、内挿アースパターンを印刷した誘電体シート５２を、その順序で積み重ね、最上部には全面に外面アースパターンを印刷した誘電体シート５１を配置する。上記の各誘電体シートの間には、必要に応じて単なる誘電体シート（導体パターンが印刷されていないシート）５０を必要枚数積層介在させる。但し、最下部の誘電体シート５６は、外側面（図２では下面）に外面アースパターンと外部入出力電極パターンが現れる向きで積層する。そして、全体を加圧することにより圧着一体化する。その後、チップの側面及び端面に共振器外導体と外部入出力電極となる導電材料を印刷し、焼結することによって、積層誘電体フィルタが得られる。実際には、大きな誘電体シートを用いて多数個取り方式で製

造し、圧着一体化後に縦横に切断して焼結することになる。

【００２３】誘電体フィルタとしての基本的な動作は公知の従来技術と同様であるから、それについての説明は省略する。等価回路も、図７に示すのと同様である（勿論、回路定数は従来品とは異なる）。本発明では、共振器内導体３２の帯状パターン３２ａの側縁に突出パターン３２ｂを設け、それと重なるように異層に容量結合用パターン３６を配置するために、必要な結合容量を確保でき、所定の周波数域に減衰極を入れることができる。しかも容量結合用パターン寸法を短くできるため、１／２波長共振による影響を３倍波よりも高域側に移動させることができ、それによって高調波特性が大幅に改善される。本発明において容量結合用パターンの長さは、隣接する共振器内導体の帯状パターンの中心線間隔よりも短くするのが好ましい。

【００２４】本発明品（図１に示す構造）と従来品（図７に示す構造）とのフィルタ通過特性（S_{21}）の比較を図３に示す。実線が本発明品の特性であり、破線が従来品の特性である。従来技術では、２倍波（$2\times f_0$）付近に１／２波長共振によるピークが現れるため減衰がとれない。それに対して本発明品では、十分な結合容量を確保できるために低域側の減衰極は従来品と同等としつつ、１／２波長共振によるピークを３倍波（$3\times f_0$）よりも高周波側に移動させることができ、それによって高調波特性が大幅に改善されていることが分かる。

【００２５】図４は本発明に係る積層誘電体フィルタの他の実施例を示す説明図であり、Ａは容量結合用パターン位置での水平断面を示し、Ｂはそのｘ－ｘ位置での断面を示している。容量結合用パターン６０以外は、前記実施例と同様になっているので、対応する部分に同一符号を付し、それらについての説明は省略する。前記実施例では、容量結合用パターンは多少長く、隣接する共振器内導体３２の帯状パターン３２ａ及び突出パターン３２ｂの両方と重なるように配置したが、この実施例の容量結合用パターン６０は、隣接する共振器内導体３２の帯状パターン間隔よりも短くし、突出パターン３２ｂのみと重なるように配置してある。

【００２６】このようにすると、容量結合用パターン６０が短くなる分、１／２波長共振による影響が更に高周波側にずれる。また図４のＢの断面からも分かるように、誘電体チップの内部での導体層の重なりは、どの位置で見ても２層以下となる。従って、積層差が緩和されて積層時に圧力がより一層平均にかかるようになり、誘電体シート間の圧着の信頼度を高め、工程の安定化を図ることができる。

【００２７】図５は本発明に係る積層誘電体フィルタの更に他の実施例の断面図である。容量結合用パターン６２以外は、前記実施例と同様になっているので、対応する部分に同一符号を付し、それらについての説明は省略する。容量結合用パターン６２は、図４の実施例と同様、隣接する共振器内導体３２の帯状パターン間隔よりも短くし、突出パターン３２ｂのみと重なるようにし、且つ共振器内導体３２を挟むように、積層方向の上下に配置している。図４に示すような構成では結合容量が不足する場合には、このような構成は有効である。

【００２８】本発明は、上記のようなコムライン型のみならず、インターデジタル型のフィルタにも適用できる。２段インターデジタル型フィルタの場合の一例を図６に示す。Ａは実装面を上に向けた状態での外観を、Ｂは内部の導体層のみの透視状態を示し、Ｃは容量結合用パターン位置での水平断面を示している。

【００２９】誘電体チップ７０の内部に一端開放で他端短絡の２個の共振器内導体７２を埋設し、該共振器内導体７２の片面側（図６のＡ，Ｂでは上方）に間隔をおいて内挿入出力電極７４を設ける。共振器内導体７２の反対面側（図６のＡ，Ｂでは下方）には間隔をおいて容量結合用パターン７６を設ける。また誘電体チップ７０の外表面に外部アース導体となる共振器外導体８０と、外部入出力電極８２を形成する。ここで共振器内導体７２は、誘電体チップ７０の一方の側面からそれに対向する他方の側面まで達するように、互いにほぼ平行に設けられ、一端が開放状態（共振器外導体８０に接続されていない）であって、他方が短絡状態（共振器外導体８０に接続されている）となっている。２個の共振器内導体７２は、開放端と短絡端とが互いに逆になるように（即ち、互い違いとなるように）設けられる。外部入出力電極８２は、前記開放端あるいは短絡端のある側面とは異なる両端面に形成され、そこから一方の主表面（図６のＡでは上面）まで延設されている。

【００３０】共振器内導体７２は、誘電体チップ７０の一方の側面から他方の側面まで延びる帯状パターン７２ａと、該帯状パターン７２ａの側縁から隣接する共振器内導体方向に向かう突出パターン７２ｂとが連続した形状であって、隣接する共振器内導体で突出パターン７２ｂが互いに向き合うように設けられる。容量結合用パターン７６は、極く単純な矩形状であって、隣接する共振器内導体７２の互いに向き合う前記突出パターン７２ｂと重なり且つ両方の突出パターン７２ｂの間を連絡するように、共振器内導体に対して積層方向で間隔をおいて配置する。

【００３１】内挿入出力電極７４は、一端で外部入出力電極８２と連続し、共振器内導体７２に対して大面積で近接対向するようなＴ型状であり、これによって入出力結合容量を増大させ、初段結合（両端に位置する共振器内導体と外部入出力電極との結合）を強くする機能を果たす。

【００３２】上記の各実施例は、いずれも共振器内導体を２個並設した２段フィルタの例であるが、本発明は３段以上のフィルタにも適用できることは言うまでもな

い。容量結合用パターン及び突出パターンは、共振器内導体の帯状パターンの中央位置に設けているが、それに限らずどらちらかにずらせて配置してもよい。例えば開放端側にずらせば、３倍波域での特性向上が生じる傾向が見られる。

【００３３】

【発明の効果】本発明は上記のように、共振器内導体の側縁に突出パターンを設け、それと重なるように異層に容量結合用パターンを配置することで、所定の位置に減衰極を入れるために必要な結合容量を確保しつつ、容量結合用パターン寸法を短くしているため、１／２波長共振による影響を３倍波よりも高域側に移動させることができ、それによって高調波特性を大幅に改善できる。

【００３４】また容量結合用パターンを、隣接する共振器内導体の帯状パターン間隔よりも短くし、突出パターンのみと重なるように片側に配置すると、誘電体チップの内部で導体層の重なりは、どの位置で見ても２層以下となって、積層差が緩和されるため、積層時に圧力がより一層平均にかかるようになり、誘電体シート間の圧着の信頼度を高め、工程の安定化を図ることができる。

【図面の簡単な説明】

【図１】本発明に係る積層誘電体フィルタの一実施例を示す説明図。

【図２】その誘電体シートの積層状態を示す説明図。

【図３】本発明品と従来品のフィルタ特性の比較説明図。

【図４】本発明に係る積層誘電体フィルタの他の実施例を示す説明図。

【図５】本発明に係る積層誘電体フィルタの更に他の実施例を示す断面図。

【図６】本発明に係る積層誘電体フィルタの他の実施例を示す説明図。

【図７】従来の積層誘電体フィルタの一例を示す説明図。

【図８】積層誘電体フィルタの等価回路図。

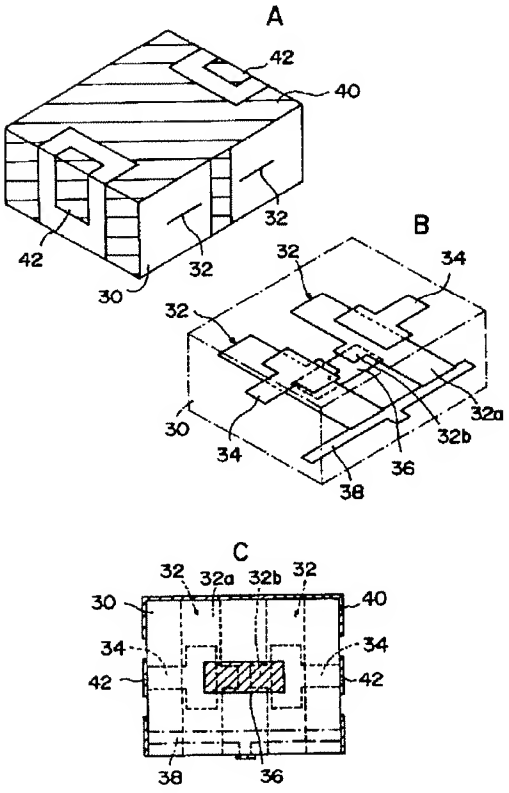
【図９】従来技術の他の例を示す説明図。

【図１０】従来技術の更に他の例を示す説明図。

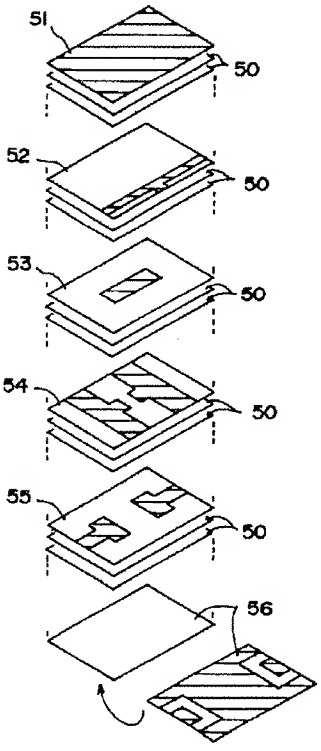
【符号の説明】

３０　誘電体チップ
３２　共振器内導体
３２ａ　帯状パターン
３２ｂ　突出パターン
３４　内挿入出力電極
３６　容量結合用パターン
３８　内挿アースパターン
４０　共振器外導体
４２　外部入出力電極

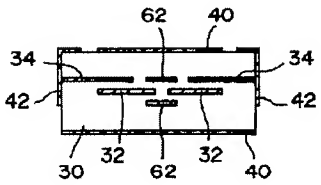
【図１】



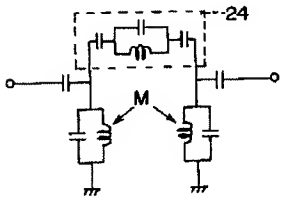
【図２】



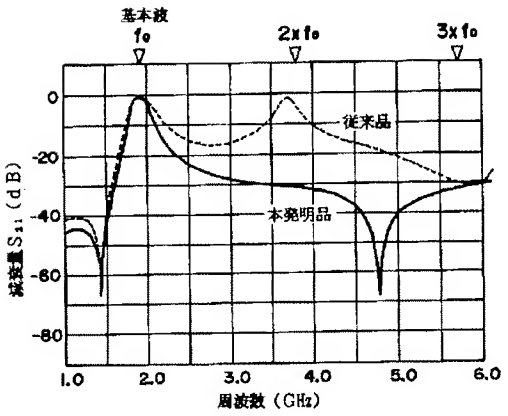
【図５】



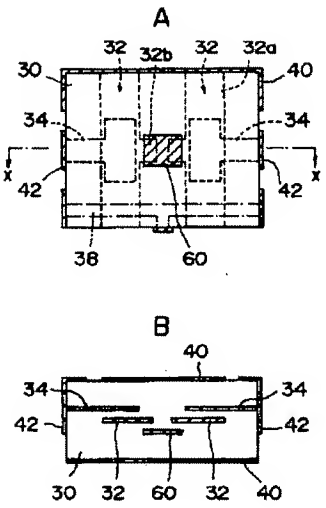
【図８】



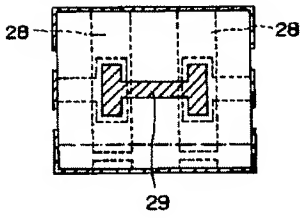
【図３】



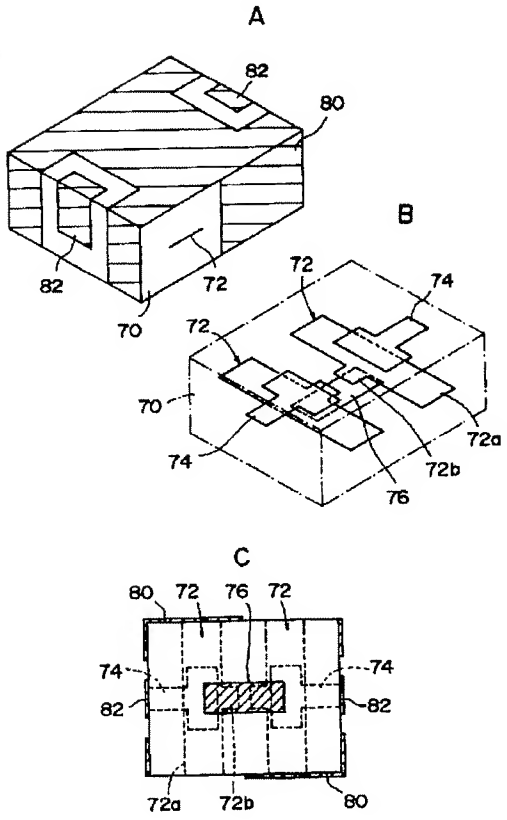
【図４】



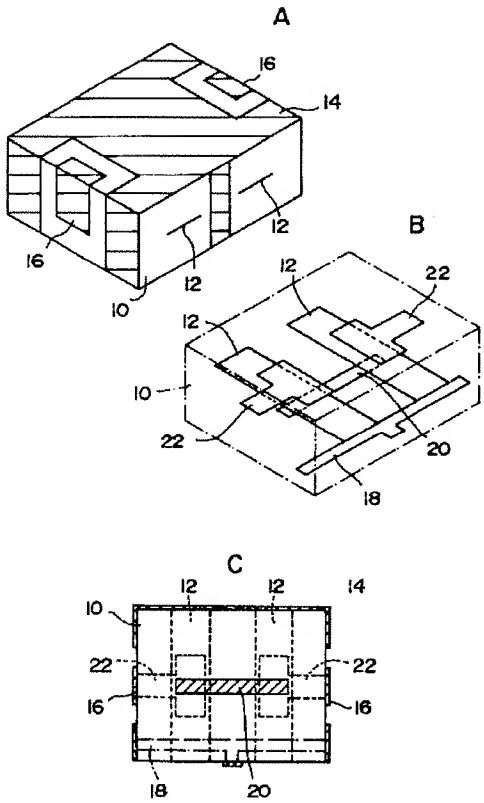
【図１０】



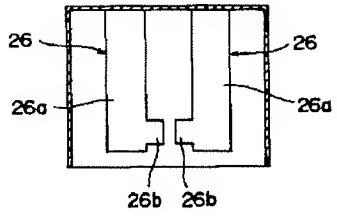
【図６】



【図７】



【図９】



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